UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/866,286	05/25/2001	Tetsujiro Kondo	450100-03242	4616

20999 7590 11/16/2006

FROMMER LAWRENCE & HAUG
745 FIFTH AVENUE- 10TH FL.
NEW YORK, NY 10151

EXAMINER	
RYMAN, DANIEL J	

ART UNIT	PAPER NUMBER
2616	

DATE MAILED: 11/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/866,286	KONDO ET AL.	
	Examiner	Art Unit	
	Daniel J. Ryman	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see Response, filed 10/20/2006, with respect to the rejection(s) of claim(s) 1-8 under 35 U.S.C. 112, second paragraph, have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Jha (USPN 6,771,663) in view of Muller et al. (USPN 6,453,360).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jha (USPN 6,771,663) in view of Muller et al. (USPN 6,453,360).

4. Regarding claim 1, Jha discloses a signal processing apparatus for receiving a time divisional multiplexed signal including a plurality of kinds of data, said signal processing apparatus comprising: switching-signal generating means for identifying a type of each of a plurality of kinds of data received as part of said time divisional multiplexed signal (where the apparatus, after receiving a packet, determines a packet type indicating a type of data contained in the packet based on a packet identifier, col. 5, lines 59-64, and where the packet is received in a TDM signal, i.e. a SONET/SDH signal, col. 1, lines 29-33, see also col. 8, lines 50-56) wherein said identification is based on information in a header of said time divisional multiplexed signal

(col. 9, lines 31-34, where identification information is based on information in the payload header of the TDM signal), said switch signal generating means generating a signal containing the type of data (col. 12, lines 2-5, where it is implicit that a signal for indicating a packet type is generated in order to allow the system to determine how to process the packet); processing means for executing one of a plurality of functional operations corresponding to the type of data of said time divisional multiplexed signal (col. 12, lines 2-5, where the packet is processed by "standard logic for handling the individual packet type," which is "processing means for executing one of a plurality of functional operations corresponding to the type of data").

Jha does not expressly disclose memory means for storing each of said plurality of kinds of data to one of a plurality of memory areas according to the identified type; processing means for executing one of a plurality of functional operations corresponding to the type of data of said time divisional multiplexed signal read from said plural memory areas at certain timing; memory input/output control means for selecting the area for storage in said memory means of a type of data in accordance with its identified type, retrieving from said memory means the stored data to be read by said processing means and supplying to said memory means data generated by said processing means after execution of one or more of the plurality of functional operations; and changing means for changing the operation of said processing means to one of said plurality of functional operations, corresponding to the type of data at the timing of the transit of said data to the processing means. However, Jha does disclose processing multiple types of packets (col. 11, lines 45-50). Muller teaches, in a system for processing packets, having memory means for storing each of said plurality of kinds of data to one of a plurality of memory areas according to the identified type (col. 5, lines 43-45, where a packet is stored in a particular buffer based on its

opcode, where the opcode is determined by the packet type, see also col. 5, lines 15-17); processing means for executing one of a plurality of functional operations corresponding to the type of data read from said plural memory areas at certain timing (col. 4, lines 24-31, where the processor processes a batch of packets of the same type before processing a batch of packets of another type in order to improve efficiency in the system, see also col. 3, lines 15-28); memory input/output control means for selecting the area for storage in said memory means of a type of data in accordance with its identified type, retrieving from said memory means the stored data to be read by said processing means (col. 5, lines 40-53, where the DMA engine controls access to the memory); and changing means for changing the operation of said processing means to one of said plurality of functional operations, corresponding to the type of data at the timing of the transit of said data to the processing means (col. 4, lines 24-31, where it is implicit that the system changes the operation when it receives a new batch of packets that are to be processed by a different protocol stack, see also col. 3, lines 16-28). Muller performs these steps in order to efficiently process packets (col. 3, lines 25-28). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the processing of TDM signals of Jha with the processor system of Muller in order to obtain a system that efficiently processes TDM signals.

Jha in view of Muller suggests supplying to said memory means data generated by said processing means after execution of one or more of the plurality of functional operations. Jha teaches that a packet that has been received and processed is then transmitted (col. 5, lines 59-61). Jha also teaches that the packets are stored in a single transmit/receive queue (col. 12, lines 49-50). It is implicit that Jha uses only a single memory for transmit/receive operations since this

is more efficient than using two separate memories. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to supply to the memory means data generated by the processing means after execution of one or more of the plurality of functional operations since only a single memory stores pre-processed packets and post-processed packets in Jha.

5. Regarding claim 2, Jha in view of Muller discloses that said processing means provides an output generated by said processing means to an input terminal of a device corresponding to each kind of the data of said time divisional multiplexed signal (Jha: Figs. 5 and 6, where the apparatus outputs to a variety of types of networks).

6. Regarding claim 3, Jha in view of Muller discloses that said processing means comprises: first data-extracting means for extracting a plurality of data as class data from said data (Jha: col. 11, lines 38-44, where the system extracts length and CRC, i.e. "class data" from the packets); characteristic signal output means for outputting a signal indicating characteristics of said class data based on said class data (col. 11, lines 45-46, where it is implicit that the system signals whether a match occurs); and generating means for generating output data based on the signal indicating the characteristics (col. 11, lines 45-50, where the payload is retrieved, i.e. output data is generated).

7. Regarding claim 4, Jha in view of Muller discloses that said processing means comprises: first data-extracting means for extracting a plurality of data as class data from said data (Jha: col. 11, lines 38-44, where the system extracts length and CRC, i.e. "class data" from the packets); characteristic signal output means for outputting a signal indicating characteristics of said class data based on said class data (col. 11, lines 45-46, where it is implicit that the system signals

whether a match occurs); second data-extracting means for extracting a plurality of data as generation data from said data (col. 11, lines 45-50, where payload data is extracted); storage means for storing coefficient information corresponding to the signal indicating the characteristics (Muller: col. 4, lines 24-31, where in order for the processor to process a batch of packets, the system must store "coefficient information corresponding to the signal indicating the characteristics" so that the system can correctly group the "batch," see also col. 3, lines 15-28); and generating means for generating output data by performing computation using said generation data and said coefficient information (Muller: col. 4, lines 24-31, where a batch of packets, i.e. "output data," is generated by performing computation using the generation data, i.e. extracted packets data, and the coefficient information, i.e. information detailing the type of packet).

8. Regarding claim 5, Jha in view of Muller suggests that said first data-extracting means extracts said class data based on class data forming information set in accordance with an instruction from said changing means (Muller: col. 4, lines 24-31, where it is implicit that the information used to "batch" packets is the same information used to determine how the packets will be processed).

9. Regarding claim 6, Jha in view of Muller suggests that said second data-extracting means extracts said generation data based on generation data forming information set in accordance with an instruction from said changing means (Muller: col. 4, lines 24-31, where it is implicit that the information used to extract the data to be batched by the system is the same information used to determine how the packets will be processed).

10. Regarding claim 7, Jha in view of Muller suggests that said storage means stores said coefficient information according to the type of said data, and outputs coefficient information, corresponding to the signal indicating the characteristics, from among said coefficient information corresponding to an instruction from said changing means (Muller: col. 4, lines 24-31, where the information is stored according to packet type and where it is implicit that the information is sent to the processor based on a signal generated from the device that informs the processor how to process the information).

11. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jha (USPN 6,771,663) in view of Muller et al. (USPN 6,453,360) as applied to claim 1 above, and further in view of Horton (USPN 5,969,770), of record.

12. Regarding claim 8, Jha in view of Muller does not expressly disclose that said plurality of functional operations are noise and luminance adjusting. Horton teaches, in a packet communication system, transporting luminance and noise information over a packet network and then processing these packets to produce a television signal (col. 4, line 41-col. 5, line 14). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the plurality of function operations include noise and luminance adjusting in order to permit the transmission of a television signal over a packet network.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel J. Ryman whose telephone number is (571)272-3152. The examiner can normally be reached on Mon.-Fri. 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571)272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Daniel J. Ryman
Examiner
Art Unit 2616

Daniel Ryman

HUY D. VU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600